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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,057	07/15/2003	Aritharan Thuraijartnam	02-4456/1P	7679
24319	7590	07/27/2004	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 LEGAL MILPITAS, CA 95035			CHAN, EMILY Y	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,057	THURAIRAJARATNAM ET AL.	
	Examiner	Art Unit	
	Emily Y Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10, 14-23 and 27 is/are pending in the application.
- 4a) Of the above claim(s) 11-13 and 24-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 14-23 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims status

Claims 11-13 and 24-26 are cancelled

Claims 1-10, 14-23, and 27 remain for examination

Claim Objections

Claims 14 and 27 are objected to because of the following informalities: "the test head " recited in claims 14 and 27 lack antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 10, 14-20, 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Goto Nobumasa et al ('2002-148291) and Bottman ('5633801).

1. With respect to claims 1, 3, 14-15, 17 and 27, Hembree et al ('848) expressly teach a semiconductor probe card having resistance measuring circuitry (see Fig 3) and a method for measuring package interconnect impedance (resistivity contact) (see Col. 2, lines 53-56) as claimed, comprising:

a tester (26) which includes a test head (30);

a device under test (DUT)/load board (10 and 12 and see Col. 4, lines 10-25) which is configured to retain a substrate (40 see Fig. 4 and Col. 6, line 44), and has signal wires which is connected to the tester (26).

Hembree et al ('848) further teach using post processing software (see Fig. 7) to analyze the data and provide interconnect impedance (resistance) versus time data.

Hembree et al ('848) do not specify using the tester (26) to store data in a file, however, Hembree et al ('848) disclose that their resistivity measuring circuit 38 can be included in a conventional digital meter contained within the tester (26) (see Col. 7, lines 52-55). Since the digital meter includes data storage or memory is well known in the art, Hembree et al ('848) 's digital meter meets the claimed feature that the tester (26) is configured to store data in a file, wherein the data is useable to obtain interconnect impedance versus time data.

Hembree et al ('848) do not teach that their tester (26) is connected to a Digital Sampling Oscilloscope (DSO) for obtaining a waveform from the Digital Sampling Oscilloscope (DSO).

Goto Nobumasa et al ('2002-148291) disclose a measuring instrument (Fig. 1) for characteristic impedance and particularly teach a Digital Sampling Oscilloscope (TDR meter 2) which is connected to a tester (probe 4) and is configured to launch a signal received by the substrate (DUT 5) and to receive a reflected signal from the substrate (DUT 5) to the tester (probe 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Goto Nobumasa et al ('2002-148291) 's TDR into Hembree

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et al ('848)'s system for the purpose of using the TDR connected to the DUT and to the tester for the expected benefit of efficiently taking the impedance measurement as disclosed by Goto Nobumasa et al ('2002-148291) (see abstract: PROBLEM TO BE SOLVED).

2. With respect to claims 2 and 16, Hembree et al ('848) teach a probe card (20) mounted to the tester (26) for contacting the substrate (40).

3. With respect to claims 4 and 18, Hembree et al ('848) teach that their probe card (20) is mounted to the tester head (26).

4. With respect to claims 5 and 19, Hembree et al ('848) teach that their probe card (20) has probe pins (22).

5. With respect to claims 6 and 20, Hembree et al ('848) teach that their probe pins (22) from the probe card (20) make contact with bump pads (44) on the substrate (see Col. 6, lines 17-23).

6. With respect to claims 8 and 22, Goto Nobumasa et al ('2002-148291) teach a coaxial cable (3) that connects the TDR to a test head (probe 4).

7. Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of Goto Nobumasa et al ('2002-148291) as applied to claims 1 and 15 respectively above, and further in view of Shahriari et al ('006).

Hembree et al ('848) in view of Goto Nobumasa et al ('2002-148291) do not disclose a socket, which is configured to hold the substrate for test.

Shahriari et al ('006) disclose a test socket system (see Fig 1a) and expressly teach a socket (106) wherein a package electronic circuit is mounted in a socket (106) for testing (see Col. 2, lines 47-48).

It would have been obvious to one of ordinary skilled in the art to incorporate the teaching of Shahriari et al ('006) 's socket (106) into Hembree et al ('848) and Goto Nobumasa et al ('2002-148291)' s system so that a test socket is used to hold the substrate for test in order to provide more accuracy testing of electrical characteristics as disclosed by Shahriari et al ('006) (see Col.1 BACKGROUND).

8. Claims 9 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al ('848) in view of in view of Goto Nobumasa et al ('2002-148291) as applied to claims 1 and 15 respectively above, and further in view of Ayadi ('748).

Hembree et al ('848) in view of in view of Goto Nobumasa et al ('2002-148291) do not teach a GPIB cable that connects the TDR to the tester.

Ayadi ('748) discloses a graphical user interface for testing integrated circuit (see Fig. 1) and expressly teach a coaxial cable (21) (see page 2, paragraph 0026, line 2) which connects the DSO (test instrument 13) to the probe card (20) and a GPIB cable (22) (see page 3, paragraph 0041, line 6-8) which connects the DSO (test instrument 13) to the tester (computer 23).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Ayadi ('748) 's coaxial and GPIB cables into Hembree et al ('848) and Goto Nobumasa et al ('2002-148291)' s system so to ensure the communication between the

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test instruments and the tester or computer as disclosed by Ayadi ('748) (see page 3, paragraph 0042, lines 9-10).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Bottman ('801) discloses that a pulse-based measurements of impedance may be performed by a time reflectometer (TDR) in a manner well known in the art (see Col. 2, lines 11-34).

Response to Amendment

Applicant's arguments with respect to claims 1-6 10, and 15-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

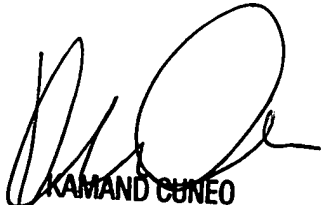
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y Chan whose telephone number is 5712721956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 5712721957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ec
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SUPERVISORY PATENT EXAMINER
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